PANCUN®

产品承认书

(APPROVAL SHEET)

公司名称 (Company)：	深圳市磐存科技有限公司
磐存料号 (PANCUN P/N)：	PCD4U16G32S48WT
产品名称 (Part Description)：	DDR4 UDIMM 3200 16GB
芯片厂商 (Chip brand)：	Samsung
芯片型号 (Dram P/N)：	K4A8G085WC-BIWE
日　　期 (Date)：	2022/11/25

Revision History

Revision	Draft Date	History	Author
1.0	2022/11/25	New release	Migo.Huang

Product Overview

DRAM Type	DDR4	Module Capacity	16GB
Module Type	UDIMM	IC Brand	Samsung
Speed	3200	CAS Latency	22
Voltage	1.2V	Operating Temp	-40°C to 85°C
Component	1Gx8	Module Rank	Dual Rank
Pin Count	288pins	ECC	No

1. INTRODUCTION

1.1. General Description

The PANCUN's memory modules are follow JEDEC standard 288-pin DDR4 SDRAM DIMMs (Unbuffered Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These DDR4 SDRAM Unbuffered DIMMs are intended for use as main memory when installed in systems such as embedded systems and industry computing. It is suitable for easy interchange and addition.

2. PRODUCT FEATURES

- **JEDEC standard**
- **VDD= VDDQ = 1.2V±0.06V (1.14V~1.26V)**
- **VPP=2.5V(2.375~2.75V)**
- **Programmable CAS Latency (posted CAS): 9,11,12,13,14,15,16,17,18**
- **8-bit pre-fetch**
- **With 8 internal banks for current operation**
- **DLL aligns DQ and DQS transition with CK transition**
- **On Die Termination (ODT)**
- **Average Refresh Period**
  - 7.8us (TCASE ≤ 85°C)
  - 3.9us (85°C < TCASE < 95°C)
- **DRAM operating temperature range**
  - Commercial (0°C ≤ TCASE ≤ 85°C)
  - Industrial (-40°C ≤ TCASE ≤ 85°C)
- **Asynchronous RESET Pin supported**
- **Package: 78 balls BGA- x8**
- **On Board EEPROM**

3. SPECIFICATIONS

Speed	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	Unit
CL-tRCD-tRP	15-15-15	17-17-17	19-19-19	20-20-20	
tCK(min)	0.938	0.833	0.750	0.625	ns
CAS Latency	15	17	19	22	tCK
tRCD(min)	14.06	14.16	14.25	13.75	ns
tRP(min)	14.06	14.16	14.25	13.75	ns
tRAS(min)	33	32	32	32	ns
tRC(min)	47.06	46.16	46.25	45.75	ns

4. ENVIRONMENTAL SPECIFICATIONS

4.1. Operating Temperature Conditions

Symbol	Parameter	Value	Unit	Notw
T_{OPER}	Normal Operating Temperature Range	-40~+85	°C	1,2,
	Extended Temperature Range	+85~+95	°C	1,3

Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between -40 to 85 °Cunder all operating conditions.

3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:

a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.

b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

5. ELECTRICAL SPECIFICATIONS

5.1. AC & DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Supply Voltage for DRAM Activating	2.375	2.5	2.75	V	3

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

5.2. Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Typ.	Max
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA relative to VSS	-0.3 ~ 1.5	V	1,3,
T_{STG}	Storage Temperature	-55 to + 100	‘C	1,2

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times.

6. INTERFACE

6.1. Pin Configurations (Front/Back side)

Pin	Front Side Pin	Pin	Back Side Pin	Pin	Front Side Pin	Pin	Back Side Pin
1	NC	145	NC	74	CK0_t	218	CK1_t
2	VSS	146	VREFCA	75	CK0_c	219	CK1_c
3	DQ4	147	VSS	76	VDD	220	VDD
4	VSS	148	DQ5	77	VTT	221	VTT
5	DQ0	149	VSS	KEY			
6	VSS	150	DQ1				
7	DM0_n,DBI0_n,NC	151	VSS	78	EVENT_n	222	PARITY
8	NC	152	DQS0_c	79	A0	223	VDD
9	VSS	153	DQS0_t	80	VDD	224	BA1
10	DQ6	154	VSS	81	BA0	225	A10/AP
11	VSS	155	DQ7	82	RAS_n/A16	226	VDD
12	DQ2	156	VSS	83	VDD	227	RFU
13	VSS	157	DQ3	84	CS0_n	228	WE_n/A14
14	DQ12	158	VSS	85	VDD	229	VDD
15	VSS	159	DQ13	86	CAS_n/A15	230	NC
16	DQ8	160	VSS	87	ODT0	231	VDD
17	VSS	161	DQ9	88	VDD	232	A13
18	DM1_n,DBI1_n,NC	162	VSS	89	CS1_n	233	VDD
19	NC	163	DQS1_c	90	VDD	234	NC
20	VSS	164	DQS1_t	91	ODT1	235	NC
21	DQ14	165	VSS	92	VDD	236	VDD
22	VSS	166	DQ15	93	NC	237	NC,CS3_n,C1
23	DQ10	167	VSS	94	VSS	238	SA2
24	VSS	168	DQ11	95	DQ36	239	VSS
25	DQ20	169	VSS	96	VSS	240	DQ37
26	VSS	170	DQ21	97	DQ32	241	VSS
27	DQ16	171	VSS	98	VSS	242	DQ33
28	VSS	172	DQ17	99	DM4_n,DBI4_n,NC	243	VSS
29	DM2_n,DBI2_n,NC	173	VSS	100	NC	244	DQS4_c
30	NC	174	DQS2_c	101	VSS	245	DQS4_t

31	VSS	175	DQS2_t	102	DQ38	246	VSS
32	DQ22	176	VSS	103	VSS	247	DQ39
33	VSS	177	DQ23	104	DQ34	248	VSS
34	DQ18	178	VSS	105	VSS	249	DQ35
35	VSS	179	DQ19	106	DQ44	250	VSS
36	DQ28	180	VSS	107	VSS	251	DQ45
37	VSS	181	DQ29	108	DQ40	252	VSS
38	DQ24	182	VSS	109	VSS	253	DQ41
39	VSS	183	DQ25	110	DM5_n, DBI5_n,NC	254	VSS
40	DM3_n,DBI3_n,NC	184	VSS	111	NC	255	DQS5_c
41	NC	185	DQS3_c	112	VSS	256	DQS5_t
42	VSS	186	DQS3_t	113	DQ46	257	VSS
43	DQ30	187	VSS	114	VSS	258	DQ47
44	VSS	188	DQ31	115	DQ42	259	VSS
45	DQ26	189	VSS	116	VSS	260	DQ43
46	VSS	190	DQ27	117	DQ52	261	VSS
47	CB4, NC	191	VSS	118	VSS	262	DQ53
48	VSS	192	CB5,NC	119	DQ48	263	VSS
49	CB0,NC	193	VSS	120	VSS	264	DQ49
50	VSS	194	CB1,NC	121	DM6_n,DBI6_n,NC	265	VSS
51	DM8_n,DBI8_n,NC	195	VSS	122	NC	266	DQS6_c
52	NC	196	DQS8_c	123	VSS	267	DQS6_t
53	VSS	197	DQS8_t	124	DQ54	268	VSS
54	CB6,NC	198	VSS	125	VSS	269	DQ55
55	VSS	199	CB7,NC	126	DQ50	270	VSS
56	CB2,NC	200	VSS	127	VSS	271	DQ51
57	VSS	201	CB3,NC	128	DQ60	272	VSS
58	RESET_n	202	VSS	129	VSS	273	DQ61
59	VDD	203	CKE1	130	DQ56	274	VSS
60	CKE0	204	VDD	131	VSS	275	DQS7
61	VDD	205	RFU	132	DM7_n,DBI7_n,NC	276	VSS
62	ACT_n	206	VD	133	NC	277	DQS7_c
63	BG0	207	BG1	134	VSS	278	DQS7_t
64	VDD	208	ALERT_n	135	DQ62	279	VSS
65	A12/BC_n	209	VDD	136	VSS	280	DQ63

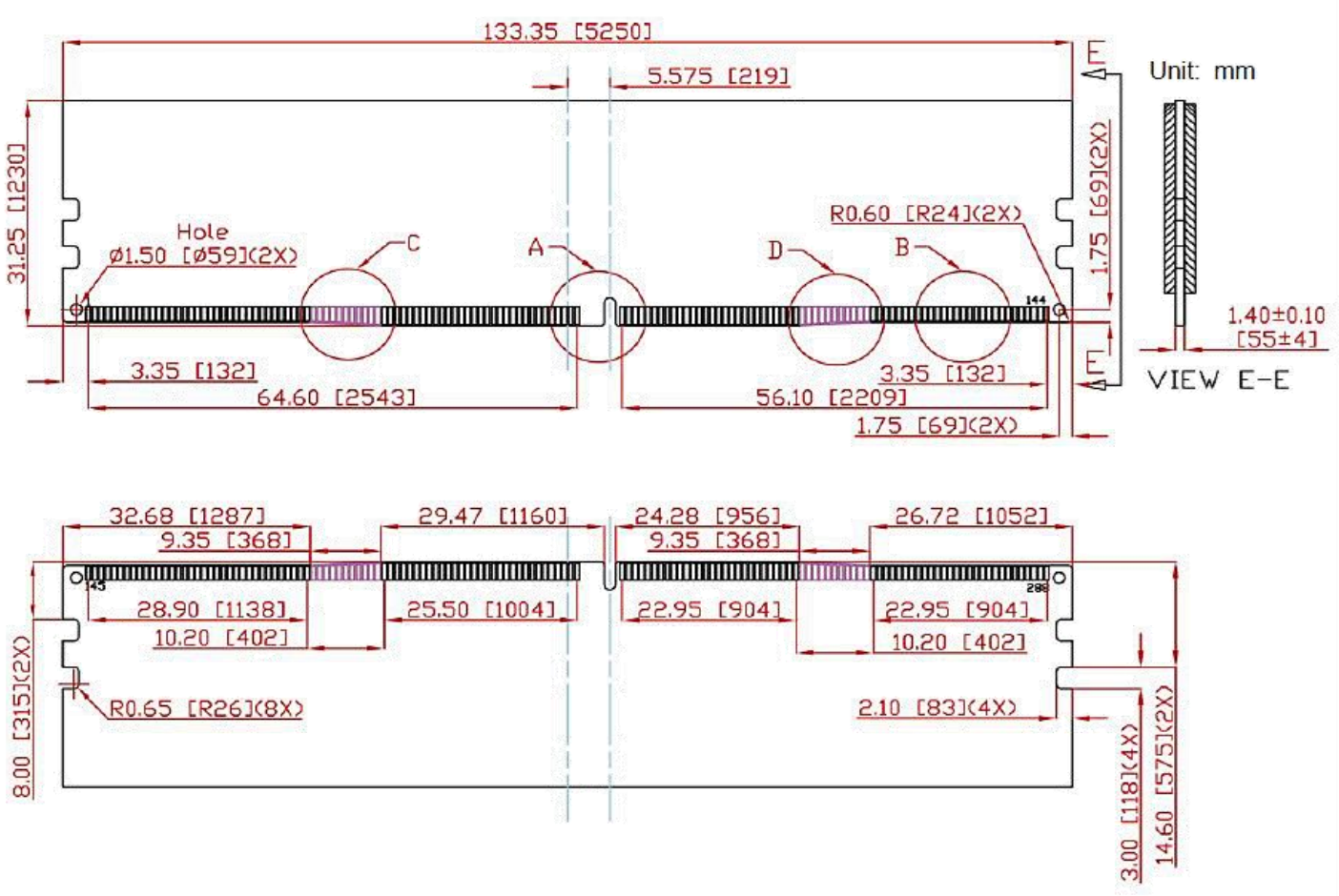
66	A9	210	A11	137	DQ58	281	VSS
67	VDD	211	A7	138	VSS	282	DQ59
68	A8	212	VDD	139	SA0	283	VSS
69	A6	213	A5	140	SA1	284	VDDSPD
70	VDD	214	A4	141	SCL	285	SDA
71	A3	215	VDD	142	VPP	286	VPP
73	A1	216	A2	143	VPP	287	VPP
73	VDD	217	VDD	144	RFU	288	VPP

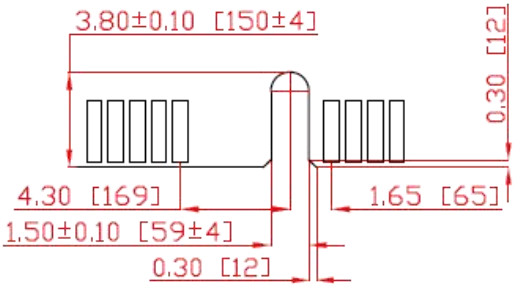
6.2. Pin Descriptions

Pin Name	Description	Pin Name	Description
A0-A17	SDRAM address bus	SCL	Serial bus clock for SPD
BA0, BA1	SDRAM bank select	SDA	Serial bus data line for SPD
BG0, BG1	SDRAM bank group select	SA0-SA2	Slave address select for SPD
RAS_n	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n	SDRAM column address strobe	VDD	SDRAM I/O and core power supply
WE_n	SDRAM write enable	VREFCA	SDRAM command/address reference supply
CS0_n, CS1_n	DIMM Rank Select Lines		
CKE0, CKE1	SDRAM clock enable lines	VSS	Power supply return (ground)
ODT0, ODT1	On-die termination control lines	VDDSPD	Serial SPD positive power supply
ACT_n	SDRAM activate	ALERT_n	SDRAM ALERT_n
DQ0-DQ63	DIMM memory data bus	VPP	SDRAM Supply
CB0-CB7	DIMM ECC check bits	RESET_N	Set DRAMs to a Known State
TDQS0_t-TDQS8_t TDQS0_c- TDQS8_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs	DM0_n- DM8_n DBI0_n-DBI8_n	SDRAM data masks/data bus inversion (x8-based x72 DIMMs)
DQS0_t-DQS8_t	SDRAM data strobes (positive line of differential pair)	EVENT_n	SPD signals a thermal event has occurred
DQS0_c-DQS8_c	SDRAM data strobes (negative line of differential pair)	VTT	SDRAM I/O termination supply
CK0_t, CK1_t	SDRAM clock (positive line of differential pair)	RFU	Reserved for future use
CK0_c, CK1_c	SDRAM clock (negative line of differential pair)		

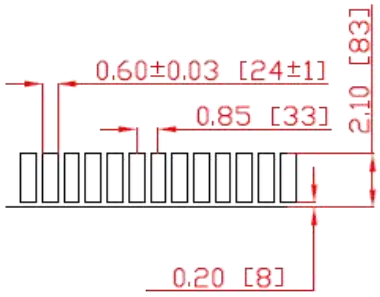
7. PHYSICAL DIMENSION

16GB,1Gbx8 as 2 ranks





Detail A



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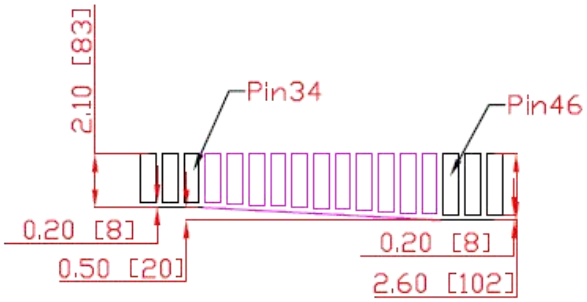

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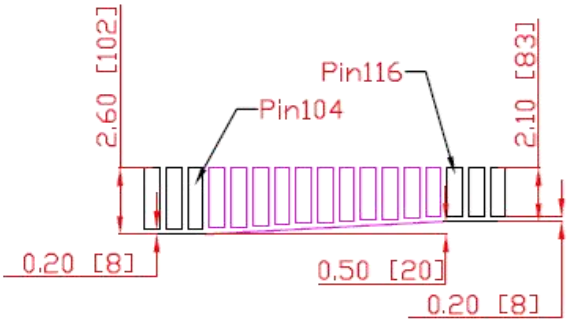

Detail D

Tolerances: ± 0.15mm unless otherwise specified

units:millimeters